CodeTAP* for i960® Hx Processor Series

- Real-Time, C/C++ Source-Level Debugging Tool for Software Engineers
- Supports Entire i960® Hx Processor Series on One CodeTAP With One Debugger
- Fully Transparent Operation at 75 MHz
- 1 Mbyte Overlay Available
- Hardware and Software Breakpoints
- 8K Trace
- CPU Browser*: Graphical Internal Register Configuration and Control Tool
- Profile and Code Coverage Support for Optimizing Compilers
- Seamless Networking Support for Workstations and PCs
- Same Intuitive Source-Level Debugger Interface as CodeICE and EL3200
- Supports Intel, MRI and GNU Compilers

CodeTAP* 960 Hx uses custom ASIC technology and patented engineering to provide all the features software engineers need to speed products to market while maintaining development schedule and staying within budget. Offering true transparency, CodeTAP requires no code modifications and does not consume target memory, communications resources, I/O locations or interrupt vectors.

CodeTAP supports all i960® H-series processor-specific features such as Big-Endian byte ordering, caching, different access modes and bus widths with no-compromise performance–like 75 MHz internal and 40 MHz external bus speeds. CodeTAP 960 Hx also supports the entire H-series with a CodeTAP unit and debugger. The emulator operates from a Sun SPARC or HP workstation, and from a PC-hosted network. It can also be accessed from a PC through a high-speed serial interface.

Execution trace history helps analyze software performance under real-time conditions. The 8K trace buffer captures the flow of instruction events during code execution

at full processor speed even when caches are enabled. A 1 Mbyte overlay memory option is available to download stable memory for debugging ROM-based code or to replace target memory. Six hardware execution, six hardware access breakpoints and 128 software breakpoints are available to track and isolate bugs. The CodeTAP Ethernet communications interface offers design teams a completely networked development solution, with no need for remote debugging operations. CPU Browser*, a graphical interface for configuration, display and modification of the states of internal processor registers and convenient profiling and code coverage support for use with Intel's optimizing C compilers is provided to enhance productivity.

Included with CodeTAP 960 Hx is the MWX-ICE C/C++ debugger environment. MWX-ICE lets you graphically organize your approach to development so you can work more easily and efficiently. You can display source code, synchronized bus-level and disassembled trace, processor

registers and other information in a multi-windowed environment customized to suit you. MWX-ICE and CodeICE can run standalone or integrated with the MasterWorks environment from Microtec Research.

HOST SYSTEMS SUPPORTED:
PC, Sun SPARC, HP 9000/700

PROCESSORS SUPPORTED:
i960 HA, HD, HT Processors

AVAILABILITY:
Q1 '96

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